Amendments to the Claims:

A listing of the entire set of pending claims (including amendments to the claims, if any) is submitted herewith per 37 CFR 1.121. This listing of claims will replace all prior versions, and listings, of claims in the application.

Listing of Claims:

1-4. (Canceled)

5. (New) A method of performing calculations and data transfers, comprising:

performing arithmetic operations in a processor substantially continuously, the arithmetic operations including functional operations and dummy operations,

transferring data between the processor and a first register, the data including select data associated with the functional operations and dummy data associated with the dummy operations,

selectively transferring the select data between the first register and a second register, and

transferring the select data between the second register and an other component,

wherein the dummy operations are performed during gaps in the functional operations so as to mask the power consumption associated with the functional operations.

6. (New) The method of claim 5, wherein

transferring the select data between the second register and the other component is performed at a time that is uncorrelated with performing the functional operations, so as to prevent a determination of a correlation of power consumed while performing the functional operations and power consumed while transferring the select data between the second register and the other component.

7. (New) The method of claim 5, wherein

the functional operations correspond to a cryptographic algorithm.

8. (New) The method of claim 5, wherein

performing the arithmetic operations, transferring the data, and transferring the select data are arranged to substantially mask power consumption related to performing the functional operations.

9. (New) The method of claim 5, wherein

performing the arithmetic operations, transferring the data, and transferring the select data are arranged to consume substantially uniform power consumption.

10. (New) An integrated circuit comprising:

a processor,

a first data register that is coupled to the processor,

a second data register that is coupled to the first data register and is configured to transfer data between the first data register and the second data register and between the second data register and an other component, and

a controller,

wherein

the processor is configured to:

perform a given set of functional operations to execute an intended algorithm during a first time sequence, and

transfer data between the processor and the first data register while performing the given set of functional operations; and

the controller is configured to control the transfer of data at the second register in a second time sequence that is substantially uncorrelated with the first time sequence, so that a correlation of first currents associated with performing the given set of functional operations and second currents associated with performing the data input and data output transfers related to the given set of functional operations cannot be determined.

11. (New) The integrated circuit of claim 10, wherein

the processor is further configured to execute dummy operations that do not affect the select data during gaps in the first time sequence.

12. (New) The integrated circuit of claim 11, wherein

the controller is further configured to control the processor to perform the dummy operations during the gaps in the functional operations.

13. (New) The integrated circuit of claim 12, wherein

the controller is configured to control the processor and to transfer the data so as to substantially mask power consumption variations related to the functional operations.

14. (New) The integrated circuit of claim 12, wherein

the controller is further configured to transfer dummy data that does not affect the select data between the first register and the second register.

15. (New) The integrated circuit of claim 14, wherein

the controller is configured to control the processor and to transfer the data so as to substantially mask power consumption variations related to the functional operations.

16. (New) The integrated circuit of claim 10, wherein

the intended algorithm is a cryptographic algorithm.

17. (New) An apparatus comprising:

a processor that is configured to perform a sequence of functional operations related to a set of data,

a first register that is configured to provide storage capabilities for the processor to perform the sequence of functional operations,

a second register that is configured to transfer the set of data between the processor and an other component, and

a controller that is configured to control the transfer of the set of data between the second register and the external component,

wherein

the controller is configured to provide the transfer of the set of data between the second register and the external component by controlling a transfer of the set of data between the second register and the first register, so that the processor can perform the sequence of functional operations related to the set of data, and

the controller is further configured to control the transfer of the set of data between the second register and the first register so that the transfer of the set of data between the second register and the other component is substantially uncorrelated to the sequence of functional operations performed by the processor.

18. (New) The apparatus of claim 17, wherein

the sequence of functional operations performed by the processor corresponds to a cryptographic algorithm.

19. (New) The apparatus of claim 17, wherein

the processor is further configured to perform other operations that are unrelated to the transfer of the set of data between the first register and the second register, so as to mask power consumptions related to the sequence of functional operations performed by the processor.

20. (New) The apparatus of claim 17, wherein

the processor is further configured to perform other data transfer operations that are unrelated to the transfer of the set of data between the first register and the second register, so as to mask power consumptions related to the transfer of the set of data between the first register and the second register.